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Paper

Feasibility Study of Layer Separation Using 2D Patterned Internal Laser Damage in Silicon

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Laser lift-off (LLO) technology is widely used to separate ultra-thin electronic devices and in advanced packaging but typically relies on a specialized laser-responsive layer, adding complexity. This paper presents an innovative take on stealth dicing by using a pulsed laser in a two-dimensional plane to create a separation interface without requiring a special layer, thus simplifying the fabrication process. The relationship between shear strength and laser ablation parameters was analyzed through shear force tests, with the modified layer morphology also examined. Shear strength for separation ranged from 200 to 20 MPa, with lower values achieved by reducing scanning pitch, increasing laser power, or enlarging the separated area. These findings highlight the potential of 2D stealth dicing as an LLO technique for ultra-thin devices. © 2025 The Author(s). *IEEJ Transactions on Electrical and Electronic Engineering* published by Institute of Electrical Engineers of Japan and Wiley Periodicals LLC.

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1. Introduction

Electronic devices are gradually transitioning from flat, rigid components to curved or flexible ones. The growing demand for wearable devices has accelerated the development of flexible transducers [1–3]. One direct approach is to use naturally soft materials, such as polymers and fluids [4]. However, this often results in sacrificing performance. As a result, various techniques have been developed to transform or transfer rigid microdevices onto flexible substrates while retaining their high performance [5–9]. Many of these techniques rely on etching sacrificial layers, but this approach is challenging to apply to piezoelectric MEMS devices, which have gained popularity due to their compactness, low voltage requirements, and ultra-low energy consumption. Several examples of thin-film piezoelectric layers grown on Si or other rigid substrates and then transferred to flexible substrates can be found in the literature [10–13]. The major challenge with this approach is the risk of delamination due to poor adhesion to the target substrate, underscoring the need for a more reliable method.

Recently, laser lift-off (LLO) technology has gained significant attention in the development of ultra-thin electronic devices due to its non-contact processing advantage [14]. It has been widely used in micro-LED fabrication and advanced packaging for electronic components [15–21], with companies like EVG [22], Disco [23], and TEL [24] releasing their own LLO technologies. Current LLO methods typically require a laser-responsive layer that facilitates separation when ablated. This method, while effective, introduces limitations such as additional fabrication steps and material constraints. In the case of piezoelectric devices, the laser-responsive layer typically cannot withstand the high temperatures required for piezoelectric thin-film deposition.

To overcome these challenges, we explored stealth dicing (SD) [25–28], an advanced laser-based technique that ablates substrates at arbitrary depths without needing a special absorbing layer. Unlike typical LLO technology, SD uses a high numerical aperture lens to focus the laser pulse into a condensed point, concentrating the laser energy. As a result, even when the material is transparent to the laser, the laser can interact with the material inside at the focal point by two-photon absorption, creating voids, cracks, or other damage. Also, rapid temperature increase generates an 'SD layer' through a thermal shockwave [29–31]. As the laser scans, the SD layer forms continuously, and interactions between these layers induce cracks in the material, greatly reducing the substrate's mechanical strength.

However, SD is conventionally used to dice chips into smaller pieces. In this study, the pulsed laser was used to 'cut' closely spaced lines within the Si substrate, creating a weakened plane that allows easy separation by applying shear stress [32]. This method could greatly simplify the transfer of piezoelectric devices to flexible substrates while preserving the integrity of the active device layers. For example, Fig. 1 illustrates the conceptual fabrication process of a high-performance flexible piezoelectric micromachined ultrasonic transducer (pMUT) array. The preferred methods for membrane fabrication are either custom

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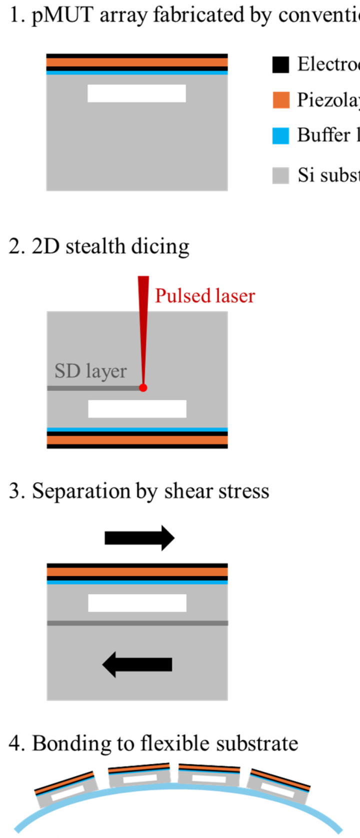

Fig. 1. Conceptual fabrication process of flexible pMUT array for wearable devices. The initial fabrication of the pMUT is done by conventional MEMS processes (Silicon-on-Nothing process is depicted [33,34]), then the proposed two-dimensional stealth dicing layer is cut to generate a weakened plane at an arbitrary height, which is later separated by the application of shear stress, and the resulting ultra-thin pMUTs are bonded to a flexible substrate

cavity SOI [35] or Silicon-on-Nothing [33,34], which provide a solid substrate for the laser processing. But backside etching is acceptable if the laser path can be aligned accurately to avoid going inside the cavities, which could damage the membranes. In this paper, shear force tests were conducted to evaluate the mechanical strength under different laser ablation parameters, and the morphology of the SD layer after laser ablation was analyzed using optical and scanning electron microscopy (SEM).

2. Experimental Methods

Figure 2 illustrates the fabrication process and experiment flow of the test samples beginning with a plain 4-in. silicon wafer (P-type, orientation [100]). The first step involved using Deep Reactive Ion Etching (DRIE) (MUC-21 ASE-SRE, Sumitomo Precision Products Co. Ltd., Japan) to form the desired square shapes. Subsequently, a pulsed fiber laser (1064 nm wavelength, pulse width 200 ns, max. average power 12 W, pulse energy 0.6 mJ, repetition frequency 20–500 kHz, model SP-12P-HS-B-B-B-B, SPI Lasers, UK) was employed to induce internal damage beneath the smooth Si surface along a two-dimensional patterned

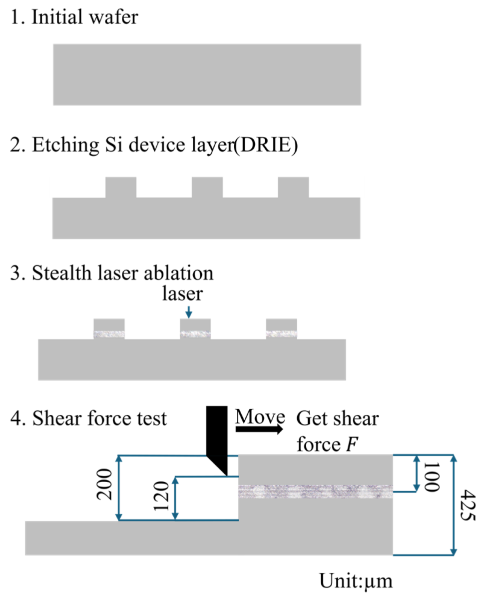

Fig. 2. Experiment flow. (1) Initial Si wafer (100) of 400 µm thickness. (2) Fabrication of square-shaped structures by DRIE. (3) Stealth laser ablation to induce easy separation. (4) Separation using a shear force measurement equipment

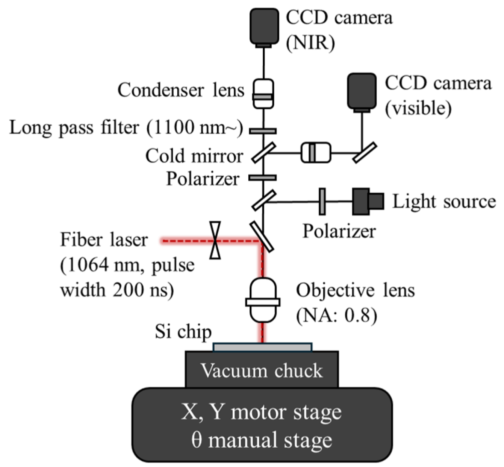

Fig. 3. Configuration of laser dicer equipment

path. The configuration of the laser dicer equipment used is shown in Fig. 3. The laser scanning pattern was a square grid with a scanning pitch ranging from 5 to 15 µm. Finally, shear force tests were conducted to evaluate the separation strength.

Figure 4 presents a series of photographs during the actual experimental process. Figure 4(a) shows the mask design used for lithography and DRIE. A thick wall was included to prevent the formation of black silicon during the DRIE process, with the square pattern sizes ranging from 100 to 500 µm, as larger sizes tend to fracture the Si substrate during the shear force test. Figure 4(b) depicts the wafer after lithography, which has an orientation of (100) and a thickness of 400 ± 15 µm. The photoresist used was PMER P-LA 900 PM (Tokyo Ohka Kogyo, Japan), which was thick enough to avoid its partial removal during the DRIE process. Figure 4(c) shows the wafer after DRIE

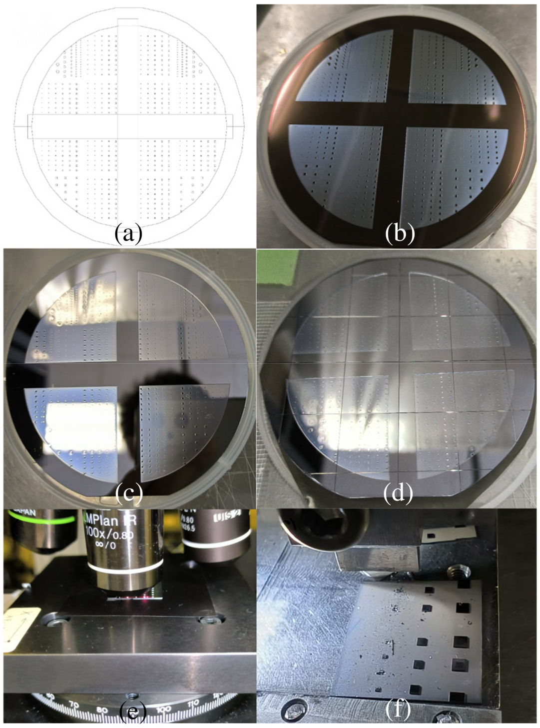

Fig. 4. Photographs of the testing sample (a) Mask design; (b) Lithography; (c) DRIE and cleaning; (d) Dicing; (e) Stealth laser ablation; (f) Shear force test

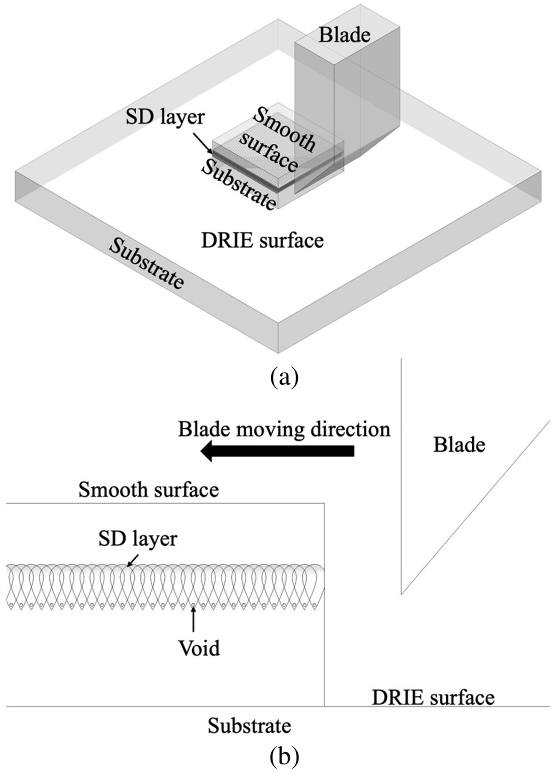

Fig. 5. Schematic diagram of (a) isometric view of the shear force test; (b) magnified cross-section view of the shear force test

and cleaning. The average height of the DRIE etching was around 200 μm. Resist removal was performed using acetone and Piranha solution (98% sulfuric acid: hydrogen peroxide = 3:1). Figure 4(d) illustrates the dicing step (DAD3240, DISCO Co., Japan), where the 4-in. wafer was divided into $2 \times 2\,\mathrm{cm}^2$ dies, as the laser dicer is limited to processing samples of this size.

Figure 4(e) displays the stealth laser ablation step using the laser dicer, which employs a × 100 IR lens to focus the laser into a very small point, estimated to have a spot diameter of about 1.6 μm, inducing internal damage within the Si. The sample stage moved freely at 2 mm/s in the $X-Y$ plane, guided by points from a CSV file, allowing for customizable laser scanning paths. Figure 4(f) captures the shear force test conducted using a Bonding Force Measurement System (PTR-1101, Rhesca Co. Ltd., Japan), where the shear force, F, required to separate each pattern was measured. After dividing by the pattern size, the shear stress (τ) was calculated, providing crucial data for evaluating mechanical strength and optimizing laser scanning pitches and other processing parameters.

A detailed schematic diagram of the shear force test is presented in Fig. 5. During internal laser ablation, voids with diameters between 1 and 3 μm are created by two-photon absorption and high temperatures at the laser focal point, which also generates a thermal shock wave, leading to the formation of the SD layer. As the laser scans, the SD layer continuously forms and interacts, creating internal cracks that significantly reduce the mechanical strength of the material. In the shear force test, by aligning the blade with the SD layer and applying horizontal shear force, the Si above the SD layer can be easily separated.

While the cross-sectional morphology of stealth dicing has been extensively studied [25–30], the top-view structures have not been reported. Therefore, photographs of the SD layer, substrate, and separated layer were taken and analyzed. During the imaging of the top layer, the sample is typically very small and prone to displacement following the application of shear force. To prevent this, adhesive tape is applied to the surface prior to conducting the shear force test.

3. Results and Discussion

3.1. Results Three parameters have shown distinctive effects in lowering shear strength: laser scanning pitch, laser power, and the pattern size. The scanning speed was kept constant at a maximum of 2 mm/s. The combination of parameters used is summarized in Table I. As shown in Fig. 6, the correlations between shear stress (τ) and these parameters are detailed.

Figure 6(a) presents the relationship between shear stress and laser scanning pitch, conducted with a sample size of $300 \times 300\,\mu\mathrm{m}^2$ and an average laser power of 0.146 W. The results indicate a positive correlation between shear stress (τ) and laser scanning pitch. This suggests that a denser laser path facilitates layer separation in Si. However, it also results in a longer processing time during the stealth laser ablation step.

Figure 6(b) is conducted with a laser path pitch of 10 μm and a sample size of $300 \times 300\,\mu\mathrm{m}^2$. The shear stress decreases rapidly as the laser power increases from 0.146 to 0.252 W. Beyond this value, the reduction in shear stress becomes less pronounced. In practical experiments, laser power above 0.557 W is hazardous, while intensities around 0.045 W or lower are insufficient to damage silicon. Therefore, a laser power of 0.252 W is recommended.

Figure 6(c) illustrates an experiment conducted with a laser power of 0.146 W and a laser path pitch of 10 μm. The shear stress exhibits a negative correlation with pattern size, suggesting

Table I. Summary of parameters used in the experiments

Parameter	Value				
Scanning pitch (μm)	5		10*		15
Average laser power	~0.146 W*	~0.252 W	~0.557 W	~0.889 W	~1.222 W
Pattern size (μm^2)	100 × 100	200 × 200	300 × 300*	400 × 400	500 × 500

*Default value when varying other parameters.

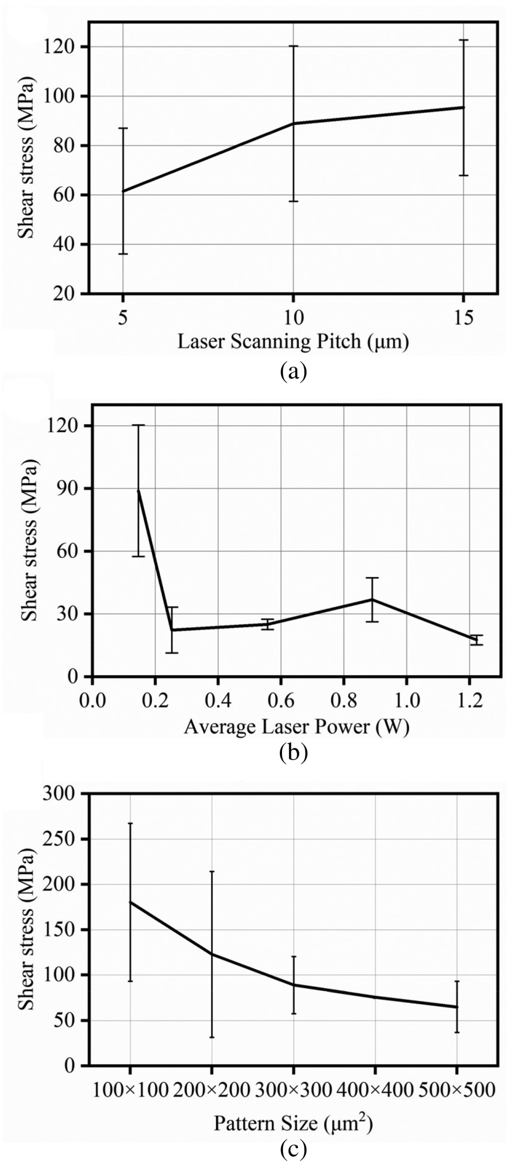

Fig. 6. Relationship between the shear stress and (a) laser scanning pitch (μm); (b) average laser power (W); (c) pattern size (μm^2)

that larger patterns are easier to separate. However, any pattern with a side length greater than 500 μm is likely to cause substrate breakage during the shear force test.

Figure 7 presents a selection of optical and scanning electron microscopy (SEM; SU-70, Hitachi, Japan) images of the tested samples. Figure 7(a) illustrates the effect of laser ablation on the smooth Si surface, showing significant morphological changes from left to right. This variation was due to slight height differences in either the sample or the stage, resulting in varied interactions of the SD layer. Figure 7(b) depicts the texture of the SD layer on the substrate after the shear force test, where the top layer has been completely removed, revealing a distinct laser scanning path. Figure 7(c) provides a magnified view of the laser-ablated layer on the substrate after the shear force test, clearly showing the presence of voids. Figure 7(d) shows the separated top layer, which was collected during the shear test using tape. The border of this layer was slightly damaged, but the central part remained intact, demonstrating the theoretical feasibility of developing a separation technology for transferring ultra-thin electronic devices.

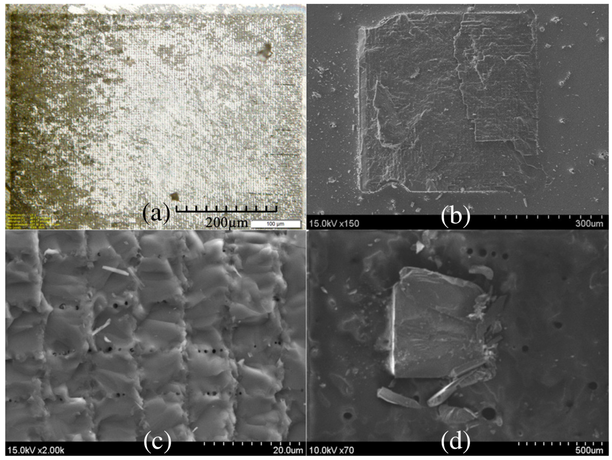

Fig. 7. Microscopic images of (a) smooth silicon surface after laser ablation, (b) substrate after the shear force test, (c) magnified substrate after the shear force test, and (d) the separated layer on top

3.2. Discussion

The shear stress required to separate the patterns from the substrate was below 200 MPa for most conditions, and it could get to a minimum of 13.1 MPa by increasing the laser power. Typical metal-to-metal bonding shear strength is several tens of MPa or higher. Therefore, a shear strength of 13.1 MPa is a result of the SD layer. On the other hand, this shear strength is still too high to separate the device without damage. As a reference, in the case of *SiC* wafer slicing, about 4.2 MPa yields good quality [36]. Based on the data from the shear force test, shear stress can be reduced by narrowing the laser scanning pitch, increasing laser power, and enlarging the pattern size. It is possible that even a lower shear strength could be obtained by using, for example, a scanning pitch of 5 μm, laser power of 0.252 W, and pattern size of 500 × 500 μm^2. It is also worth mentioning that the laser used in this study was a commercially available one and different from the one used in Disco's stealth dicers (developed by Hamamatsu

Photonics), which was specially optimized for stealth dicing. It is expected that using such a special laser can significantly reduce the shear stress for separation. Alternatively, the current setup could be optimized by increasing the NA of the objective lens, exploring other pulse durations and repetitions, or exploring other spatial distributions such as Bessel or Vortex laser. Although it is currently challenging to remove the top layer without causing damage, the results presented here indicate that it is possible.

As can be seen in Fig. 7(d), the surface is not perfectly flat and smooth. The surface quality will define which bonding methods can be used for the fabrication of flexible devices. In this work, the intended method is adhesive bonding, which could benefit from a moderately rough surface. However, alternatives such as laser welding [37] could be applied after mechanical polishing.

Future work should focus on further optimizing laser ablation parameters to identify the optimal separation conditions. Additionally, the current separation force is limited to shear force; however, applying a combination of forces, including shear, lifting, and torsional forces, could make damage-free separation more easily achievable.

4. Conclusion

The feasibility of using stealth laser dicing along a two-dimensional patterned path was investigated. The test samples consisted of Si substrate with square-shaped structures fabricated by DRIE that were then ablated by laser stealth dicing following a 2D path and finally separated using a shear stress measurement equipment. The relationships between laser scanning pitch, laser intensity, pattern size, and shear strength have been measured, and the top-view morphology of the SD layer was examined. Lower shear strengths were obtained with smaller scanning pitch, higher laser power, and bigger pattern size up to about 20 MPa. The obtained shear strengths, almost all under 200 MPa, suggest that 2D stealth laser dicing could be a viable technique for transferring ultra-thin electronic devices.

References

(1) Li Y, Li Y, Zhang R, Li S, Liu Z, Zhang J, Fu Y. Progress in wearable acoustical sensors for diagnostic applications. *Biosensors and Bioelectronics* 2023; **237**:115509.

(2) Ray TR, Choi J, Bandodkar AJ, Krishnan S, Gutruf P, Tian L, Ghaffari R, Rogers JA. Bio-integrated wearable systems: A comprehensive review. *Chemical Reviews* 2019; **119**(8):5461–5533.

(3) Yokota T, Fukuda K, Someya T. Recent Progress of flexible image sensors for biomedical applications. *Advanced Materials* 2021; **33**(19):2004416.

(4) Lin M, Zhang Z, Gao X, Bian Y, Wu RS, Park G, Lou Z, Zhang Z, Xu X, Chen X, Kang A, Yang X, Yue W, Yin L, Wang C, Qi B, Zhou S, Hu H, Huang H, Li M, Gu Y, Mu J, Yang A, Yaghi A, Chen Y, Lei Y, Lu C, Wang R, Wang J, Xiang S, Kistler EB, Vasconcelos N, Xu S. A fully integrated wearable ultrasound system to monitor deep tissues in moving subjects. *Nature Biotechnology* 2024; **42**(3):448–457.

(5) Ko HC, Stoykovich MP, Song J, Malyarchuk V, Choi WM, Yu C-J, Geddes JB, Xiao J, Wang S, Huang Y, Rogers JA. A hemispherical electronic eye camera based on compressible silicon optoelectronics. *Nature* 2008; **454**(7205):748–753.

(6) Ahn J-H, Je JH. Stretchable electronics: Materials, architectures and integrations. *Journal of Physics D: Applied Physics* 2012; **45**(10):103001.

(7) Huang K, Dinyari R, Lanzara G, Kim JY, Feng J, Vancura C, Chang F-K, Peumans P. An approach to cost-effective, robust, large-area electronics using monolithic silicon. In *IEEE International Electron Devices Meeting*. IEEE: Washington DC, USA; 2007; 217–220.

(8) Rojas JP, Arevalo A, Foulds IG, Hussain MM. Design and characterization of ultra-stretchable monolithic silicon fabric. *Applied Physics Letters* 2014; **105**(15):154101.

(9) Sung W-L, Lai W-C, Chen C-C, Huang K, Fang W. Micro devices integration with large-area 2D chip-network using stretchable electroplating copper spring. In *2014 IEEE 27th International Conference on Micro Electro Mechanical Systems (MEMS)*. IEEE: San Francisco, CA, USA; 2014; 1135–1138.

(10) Joshi SV, Sadeghpour S, Kraft M. Fabrication of high-frequency 2D flexible pMUT Array. In *2023 IEEE 36th International Conference on Micro Electro Mechanical Systems (MEMS)*. IEEE: Munich, Germany; 2023; 331–334.

(11) Joshi SV, Sadeghpour S, Kraft M. Bendable polymer-based high-frequency pMUTs on transparent SU8 and polyimide substrates. In *22nd International Conference on Solid-State Sensors, Actuators and Microsystems (Transducers)*. Kyoto, Japan; IEEE; 2023; 849–852.

(12) Pavageau F, Dieppedale C, Perreau P, Liechti R, Hamelin A, Licitra C, Casset F, Le Rhun G. Highly transparent piezoelectric PZT membranes for transducer applications. *Sensors & Actuators. A, Physical* 2022; **346**:113866.

(13) Samoto T, Hirano H, Somekawa T, Hikichi K, Fujita M, Esashi M, Tanaka S. Wafer-to-wafer transfer process of barium strontium titanate for frequency tuning applications using laser pre-irradiation. *Journal of Micromechanics and Microengineering* 2015; **25**(3):035015.

(14) Wang F, Liu Q, Xia J, Huang M, Wang X, Dai W, Zhang G, Yu D, Li J, Sun R. Laser lift-off Technologies for Ultra-Thin Emerging Electronics: Mechanisms, applications, and Progress. *Advanced Materials Technologies* 2023; **8**(7):2201186.

(15) Delmdahl R, Pätzel R, Brune J. Large-area laser-lift-off processing in microelectronics. *Physics Procedia* 2013; **41**:241–248.

(16) Delmdahl R, Fricke M, Fechner B. Laser lift-off systems for flexible-display production. *Journal of Information Display* 2014; **15**(1):1–4.

(17) Ueda T, Ishida M, Yuri M. Separation of thin GaN from sapphire by laser lift-off technique. *Japanese Journal of Applied Physics* 2011; **50**:41001.

(18) Chu C-F, Lai F-I, Chu J-T, Yu C-C, Lin C-F, Kuo H-C, Wang SC. Study of GaN light-emitting diodes fabricated by laser lift-off technique. *Journal of Applied Physics* 2004; **95**(8):3916–3922.

(19) Kim S-J, Ahn T, Suh MC, Yu C-J, Kim D-W, Lee S-D. Low-leakage polymeric thin-film transistors fabricated by laser assisted lift-off technique. *Japanese Journal of Applied Physics* 2005; **44**:L1109.

(20) Yue L, Xu J, Wang X, Zhou J, Wang Y, Yao L, Niu M, Wang M, Cao B, Xu Y, Wang J, Xu K. Flexible arrays of GaN-based micro-LEDs fabricated on different substrates by a laser lift-off process. *Japanese Journal of Applied Physics* 2024; **63**:51007.

(21) Chancerel F, Urban P, Slabbekoorn J, Halas S, Bravin J, Brems S, Uhrmann T, Wimplinger M, Phommahaxay A, Beyne E. IR laser release for 3D stacked devices: effect of the release stack structure on the debonding mechanism. In *2024 IEEE 74th Electronic Components and Technology Conference (ECTC)*. IEEE: Denver, CO, USA; 2024; 343–347.

(22) IR LayerReleaseTM Technology [Online]. https://www.evgroup.com/technologies/ir-layerrelease-technology Accessed: November 22, 2024.

(23) Rēzārifutoofu (LLO, Laser Lift-Off) kakō [Online]. https://technology.disco.co.jp/jp/method/laser-lift-off/ Accessed: January 20, 2024.

(24) Saisentan debaisu 3-jigen jissō no gijutsu kakushin ni kōken suru rēza hakuri gijutsu o kaihatsu [Online]. https://www.tel.co.jp/news/product/2023/20231211_001.html (In Japanese) Accessed: January 20, 2024.

(25) Kumagai M, Uchiyama N, Ohmura E, Sugiura R, Atsumi K, Fukumitsu K. Advanced dicing technology for semiconductor wafer – stealth dicing. *IEEE Transactions on Semiconductor Manufacturing.* 2007; **20**(3):259–265.

(26) Fujita M, Izawa Y, Tsurumi Y, Tanaka S, Fukushi H, Sueda K, Nakata Y, Esashi M, Miyanaga N. Debris-free low-stress high-speed laser-assisted dicing for multi-layered MEMS. *IEEJ Transactions on Sensors and Micromachines* 2010; **130**(4):118–123.

(27) Izawa Y, Tsurumi Y, Tanaka S, Fukushi H, Sueda K, Nakata Y, Esashi M, Miyanaga N, Fujita M. Debris-free high-speed laser-assisted low-stress dicing for multi-layered MEMS. *IEEJ Transactions on Sensors and Micromachines* 2009; **129**(3):63–68.

(28) Marks MR, Cheong KY, Hassan Z. A review of laser ablation and dicing of Si wafers. *Precision Engineering* 2022; **73**:377–408.

(29) Lim DK, Vempaty VRSP, Shah AH, Sim WH, Singh HV. Modeling of laser absorption and modification layer formation within silicon due to stealth dicing. *IEEE Transactions on Components, Packaging and Manufacturing Technology* 2023; **13**(9):1486–1493.

(30) The WH. Stealth dicing characterization, optimization, integration, and operations Management for ultra-thin stacked memory dies. M.Sc. Thesis, Massachusetts Institute of Technology, Cambridge. 2015.

(31) Wang L, Zhang C, Liu F, Zheng H, Cheng GJ. Ultrafast pulsed laser stealth dicing of 4H-SiC wafer: Structure evolution and defect generation. *Journal of Manufacturing Processes* 2022; **81**:562–570.

(32) Yao Y, Vergara A, Tanaka S. Feasibility study of layer separation using 2D patterned internal laser damage in silicon. In *37th International Microprocesses and Nanotechnology Conference (MNC 2024) 15D-2-3*. Kyoto, Japan; Japan Society of Applied Physics; 2024.

(33) Sekiguchi T, Yoshida S, Kanamori Y, Tanaka S. Epitaxial Pb(Zr,Ti)O3-based piezoelectric micromachined ultrasonic transducer fabricated on silicon-on-nothing (SoN) structure. In *2023 IEEE 36th International Conference on Micro Electro Mechanical Systems (MEMS)*. IEEE: Munich, Germany; 2023; 139–142.

(34) Sarafianou M, Choong D, Chen D, Goh D, Yao Z, Sharma J, Merugu S, Ng E, Lee J. Long-range high-resolution imaging with silicon-on-nothing ScAlN pMUTs. *IEEE Sensors Journal* 2023; **23**(20):24254–24263.

(35) Lu Y, Horsley D. Modeling, fabrication, and characterization of piezoelectric micromachined ultrasonic transducer arrays based on cavity SOI wafers. *Journal of Microelectromechanical Systems* 2015; **24**(4):1142–1149.

(36) Zhang Y, Xie X, Huang Y, Hu W, Long J. Internal modified structure of silicon carbide prepared by ultrafast laser for wafer slicing. *Ceramics International* 2023; **49**(3):5249–5260.

(37) Jia X, Luo J, Li K, Wang C, Li Z, Wang M, Jiang Z, Veiko VP, Duan J. Ultrafast laser welding of transparent materials: From principles to applications. *International Journal of Extreme Manufacturing* 2025; **3**:32001.

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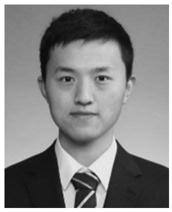

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